Advances in III-V Compounds and Solar Cells Grown on SiGe Substrates

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ABSTRACT

The use of compositionally graded SiGe buffers to bridge material mismatches between GaAs based III-V compounds and Si substrates has shown extreme promise as the means by which high efficiency III-V solar cells can be integrated with low-cost Si substrates. In this paper, we describe recent progress in three areas that are critical to realize the potential of GaAs/Ge/SiGe/Si integration for photovoltaic technologies of the future. First, we show that p^+n configured GaAs cells are much less sensitive to dislocation-related degradation than n^+p configured cells, indicating a preferred polarity for heteroepitaxial III-V solar cells. Second, by correlating direct, microscopic observation using cross sectional TEM and EBIC with sub-GaAs bandgap light I-V studies, we show that interface states present at the GaAs/Ge interface unrelated to anti-phase domains are responsible for uncontrolled sub-GaAs bandgap PV response for p^+n cells. Further, we demonstrate a solution to this problem that completely eliminates and reproducibly controls such interfacial activity. Finally, GaAs/Ge/SiGe/Si cell areas are increased from 0.36 cm^2 to 4 cm^2 without reduction of cell performance, the first experimental evidence that no fundamental limitations are evident for scaling III-V/Ge/SiGe/Si cells to large areas.

1. Introduction

The ability to epitaxially integrate optimum solar cell designs based on III-V compounds such as GaAs, InGaP, and advanced multi-bandgap structures, with cheap, abundant, large, strong and lightweight substrates such as Si would offer tremendous advantages in the power output/cost metric for photovoltaic system implementation in a variety of applications. As a result, the notion of III-V/Si integration has been explored for decades [1]. Unfortunately, the material perfection required to produce the highest performance III-V solar cells had not been achieved due to the basic differences in lattice constant and other key structural properties between the III-V solar cell materials and the Si substrate, which generate performance-limiting defects (4% lattice misfit between GaAs and Si; 60% thermal expansion mismatch). While significant efforts had been undertaken to mitigate these problems, none have achieved the breakthrough necessary to allow photovoltaic quality III-V material to be achieved over any useful area.

Recently, we have established a different approach where, by growing compositionally graded, relaxed SiGe buffers up to a composition of 100% Ge, a virtual Ge substrate with the mechanical, structural and thermal properties of Si can be substituted for conventional Ge substrates in PV technologies [2]. Other work to eliminate the formation of anti-phase domain disorder and to suppress auto-doping at the GaAs/Ge interface in GaAs/Ge/SiGe/Si heterostructures led to the demonstration of the highest reported carrier lifetimes for GaAs/Si and promising, small area GaAs/Si solar cells with high performance and record V_{oc} output [3-5]. Here we report progress in three areas critical to advance the III-V/SiGe/Si integration scheme toward technological viability: (1) determination of a fundamental cell polarity preference for any mismatched III-V cell structure; (2) identification of and solution to GaAs/Ge electrical interface activity in p^+n cells on Ge/SiGe/Si; and (3) increase of high performance GaAs/Ge/SiGe/Si cell areas to 4 cm^2. These are key issues for meeting the program objectives of demonstrating a Si-based, virtual Ge substrate technology, and exploiting the inherent SiGe bandgap engineering opportunities for achieving optimum bandgap profiles using composite III-V/SiGe heterostructures.

2. Experimental

Conventional, single junction GaAs p^+n and n^+p cells with InGaP window and BSF layers were grown on SiGe coated Si wafers following our prior publications [4,5]. Hence, details will not be presented here other than to outline the basic approach. Virtual Ge (v-Ge) substrates were generated by growth of compositionally graded SiGe layers on 6° off-cut (001) Si wafers using both LPCVD (low pressure chemical vapor deposition) and UHVCVD (ultra high vacuum chemical vapor deposition). The terminal buffer composition of 100% Ge was obtained by using an average grading rate of 10% Ge/um through the step-graded buffer. The GaAs growth was initiated on v-Ge substrates with SSMBE (solid source molecular beam epitaxy) and the III-V cell structure was completed by MOCVD (metalorganic chemical vapor deposition). MOCVD growth conditions followed our standard process for GaAs/GaAs cell growth [5]. This process has yielded threading dislocation densities of 0.8-2x10^6 cm^{-2} and minority carrier lifetimes as high as 10.5 ns in n-GaAs with no anti-phase domain (APD) disorder [4]. To evaluate the impact of interface states at the GaAs/Ge interface within the composite heterostructures, several SSMBE growth variables were systematically investigated, including the use of low temperature migration enhanced epitaxy (MEE) for

GaAs nucleation, the growth of a thin Ge epitaxial layer on the v-Ge substrate prior to growth of GaAs, and direct growth of GaAs on the graded v-Ge substrate using MEE nucleation. Sub-GaAs bandgap photo-response was measured using an in-house light I-V test equipment with a series of low pass optical filters (Si and Ge wafers). Cross sectional EBIC (electron beam induced current) and TEM (transmission electron microscopy) analysis of the interface region was accomplished by sample preparation using selective focused ion beam (FIB) milling. Cells were processed in a standard fashion using a newly designed mask set to accommodate both test diodes and cell areas from 0.25 cm^2 to 4 cm^2. Anti-reflection coatings were not applied as of this writing. Cell results are for AM0 illumination due to local availability of such tests. We are awaiting AM1.5 tests, the results of which should be available at the time of the meeting.

3. Results and Discussion

3.1. Impact of Polarity on Heteroepitaxial GaAs Cell Performance

A study to determine the applicability of virtual Ge (v-Ge) substrates for both p^+n and n^+p configured GaAs cells was undertaken to assess the universality of the v-Ge substrate approach to meet different technology needs. Figure 1 shows AM0 light I-V response for p^+n and n^+p cells grown on similar dislocation density v-Ge substrates. A substantial reduction in Voc is observed from 980 mV (AM0) for p^+n cells to 906 mV (AM0) for n^+p cells, but with similar Jsc and FF values. The reduced Voc for the n^+p cell can be understood by analyzing the dark I-V data for both types of cells, and recognizing that for GaAs, the dominant diode transport mechanism at V_{oc} is depletion region recombination within the lower doped base layers. For this transport mechanism, J_o can be expressed as:

$$J_o = 0.5qn_iW\frac{D}{L^2} = 0.5qn_iW\frac{1}{\tau}. \qquad (1)$$

Here, τ is the minority carrier lifetime within the lower doped base region. As shown in Table I, the extracted values of J_o for p^+n and n^+p cells grown on v-Ge substrates with identical TDD values are very different. The larger J_o for the n^+p structure results in the lower V_{oc} observed in Figure 1. The difference in J_o values is due to differences in minority carrier lifetimes for electrons and holes in the base-dominated depletion regions for each cell polarity. To confirm this, a series of p-type (with a nominal doping of $2x10^{17}$ cm^{-3}) InGaP/GaAs double heterostructures (DH) were grown to perform time resolved photoluminescence (TRPL) so that minority carrier electron lifetimes could be extracted. As seen in Table 1, a 2 ns minority electron lifetime in p-GaAs was obtained, as opposed to a much higher 10.5 ns minority carrier hole lifetime that was measured for n-GaAs DH structures on v-Ge with the same TDD and doping concentration. The shorter minority carrier lifetime for electrons can be understood by realizing that the much larger mobility of electrons as compared to holes in GaAs translates to an increased sampling rate of the residual defects within the material, resulting in shorter recombination lifetimes at a given TDD value, and thus a greater sensitivity of electron lifetime on TDD than for hole lifetime. Thus, the result of the low electron lifetime is to increase the base component of the depletion region recombination current for the n^+p structure as compared to the p^+n structure according to eq. 1, thereby reducing Voc. Hence, n^+p cells are far more sensitive to the residual TDD

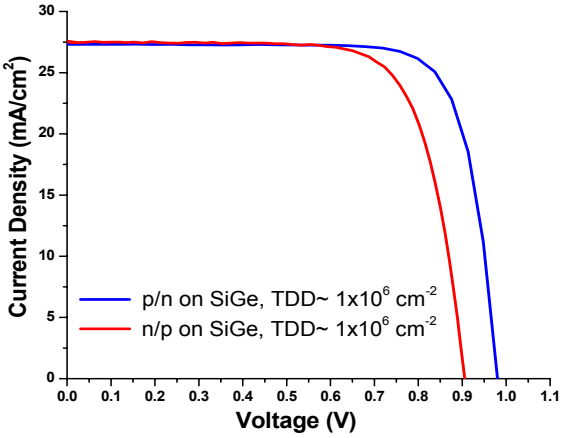

Figure 1: Illuminated AM0 I-V response for p^+n and n^+p GaAs cells grown on v-Ge substrates with close TDD values. Note the difference in Voc. The p^+n AM0 efficiency is 15.6% and the n^+p cell is 13% efficient. AM1.5 values will be ~ 2-3 absolute percent higher.

than p^+n cells, and thus require further TDD reduction to achieve highest efficiencies using conventional cell design guidelines. Details of the preliminary results can be found in a recent publication [6] and a full study of the general applicability of this finding to any lattice mismatched III-V photovoltaic device with low, but non-negligible residual TDD is the topic of an upcoming paper.

Table I. Measured values for diode ideality factor (n), minority carrier base lifetime, Jo and Voc (AM0).

parameter	p^+n	n^+p
n	2	2.2
Base minority τ (ns)	10.5	2
J_o (A/cm^2)	1.0e-9	7.0e-9
V_{oc} (mV)	980	906

3.2. Detection and Elimination of Electrical Activity at GaAs/Ge Interfaces Within GaAs/Ge/SiGe/Si Cells

An outstanding problem within the III-V/Ge photovoltaics community has been the issue of GaAs/Ge

interface states and their impact on photovoltaic properties. For n^+p GaAs cells on Ge wafers, this is less of an issue due to the use of a diffused homo-junction within Ge. For p^+n GaAs cells on Ge, the problem is more complex since inadvertent band bending resulting from interface charging can impact I-V characteristics to the extent that photo-voltages can be uncontrollably generated. To date this issue has not been explored for GaAs cells on v-Ge, where the presence of residual TDD and surface crosshatch must be evaluated in this context for eventual device implementation. Thus, a systematic study to investigate the GaAs/Ge interface electrical activity and possible sources was undertaken and is reported on here. As described in section 2, the use of MBE to initiate the III-V cell growth allows substantial control of the III-V interface formation by using MEE and a Ge epitaxial layer grown on the v-Ge substrates as variables. Table II shows Voc data measured from p^+n GaAs cells under an uncalibrated ELH bulb light source, and Voc measured after filtering the light with low pass Si optical filters. No subgap photovoltage (or photoresponse from full I-V data) is observed for cells grown using a Ge epitaxial layer on the v-Ge substrate. However, there is a clearly a sub-GaAs bandgap photo-response for the cells grown on a v-Ge wafer directly, without the Ge epilayer. This result is very reproducible and is consistent with the presence of GaAs/Ge interface states and resultant photo-responses from sub-GaAs bandgap absorption.

Table II. Voc data for p^+n cells measured using an uncalibrated white light source with and without a Si long pass filter. Calibrations using a Ge filter shows the noise floor of the measurement to be ~ 1 mV, indicating that the only sub-GaAs bandgap response is for the cell without the Ge epilayer.

Growth parameter	V_{oc} without filter (mV)	V_{oc} with filter (mV)
Ge epi MEE	900	0.4
Ge epi No MEE	860	1
NO Ge epi MEE	1060	120

The source for such interface states is the question, and to investigate the possible role of APDs, a systematic study was undertaken for GaAs layers grown on Ge wafers with and without MEE, based on the cell results of Table I. Past work by our group has shown that APD disorder can be completely eliminated, even at the nanometer scale by MEE nucleation of the initial GaAs layer on a Ge surface [3]. In addition, we have shown that by co-evaporation of Ga and As at low growth temperatures, APD formation and total, short-range (within 100 nm of the GaAs/Ge interface) APD self-annihilation can be achieved. Thus with these two growth variations we can generate a unique sample set with laterally uniform, short-range APD disorder and samples with no APD disorder down to local length scales. Figure 2 shows cross sectional TEM images of GaAs grown on Ge wafers on which the Ge epilayers were grown, but the GaAs growth was initiated with and without MEE. The presence of short range APD disorder and their elimination using MEE is indicated. Preliminary cross sectional EBIC images, which were obtained quantitatively on the same samples, do not indicate interface charging in spite of the presence of APDs, and this is consistent with cell results and the filtered light I-V responses where we do not observe any sub GaAs bandgap junction activity when the Ge epilayer is included, regardless of GaAs nucleation conditions (MEE, no MEE). For all such cells, true single junction p^+n GaAs cell characteristics on the SiGe/Si substrates is maintained, and the high AM0 Voc values of 980 mV are confirmed to be from the single junction.

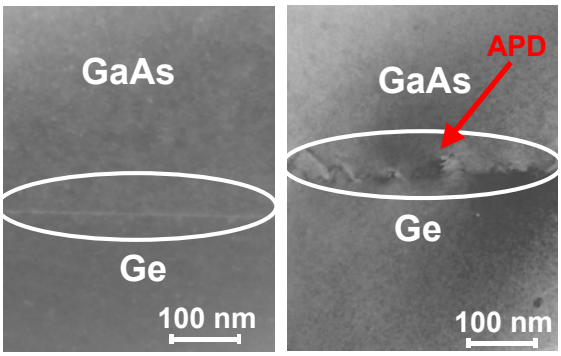

Figure 2. Cross sectional TEM images of GaAs/Ge epilayer interfaces, with (left) and without (right) an MEE GaAs nucleation step.

As seen from Table II, the interface between GaAs and the v-Ge surface is clearly a source of photo-response for cells grown on v-Ge without a pre-GaAs growth Ge epitaxial layer. The ~ 120 mV photo-voltage measured from the GaAs/v-Ge interface using the filtered light illumination experiment increases the p^+n cell Voc to ~ 1060 mV for the particular cell listed in the table. Subtraction of the interface photovoltage results in a Voc of ~ 940 mV, a value consistent with the range of Voc values observed for true single junction GaAs cells on the v-Ge substrates with a TDD of ~ $1x10^6$ cm^{-2}. The physical source(s) for the GaAs/v-Ge interface activity is currently being investigated. The lack of correlation with the interface photoresponse and APD disorder suggests that impurities at the GaAs/v-Ge interface may be the source, and further investigations are ongoing. Regardless of the source, we have demonstrated a solution to the problem of interface activity by growth of a thin Ge epitaxial layer on the v-Ge substrate prior to III-V growth.

3.3. Large Area GaAs Cells on Si Using SiGe Buffers

Past GaAs/Si solar cells have been very limited in total areas, due primarily to thermal expansion coefficient mismatches that generate tensile stress leading to wafer bow or cracks for larger area and thicker solar cells. An advantage of the SiGe grading process employed in our v-Ge substrate approach is that the compressive strain inherent in the compositionally graded alloy from Si to Ge can be used to balance the thermally-induced tensile strain during growth cooldown that results from thermal expansion mismatch between Ge and Si. This thermal cycle (which reduces, but does not necessarily eliminate microcrack formation) and the presence of crosshatch on the v-Ge substrate prior to III-V growth may enhance or alter the accommodation of additional tensile stress that can accumulate during subsequent III-V overgrowth to form the III-V/SiGe/Si composite heterostructure. While this is a topic of current focus by our group, we have recently achieved high performance, large area GaAs cells on Si using the v-Ge approach.

Figure 3 shows light I-V characteristics for p+n GaAs/v-Ge cells with areas of 0.36 cm^2, 1 cm^2 and 4 cm^2, without benefit of an antireflection coating that provides a

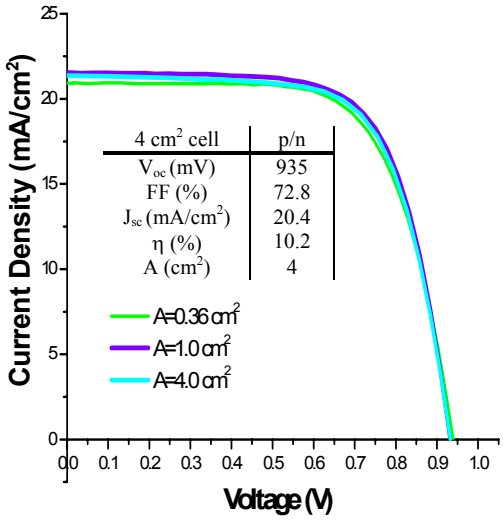

Figure 3. AM0 I-V data for GaAs/v-Ge cells with areas of 0.36 cm^2, 1 cm^2 and 4 cm^2. Inset shows total area cell data for the 4 cm^2 cell (7% grid coverage). No AR coatings have been applied.

current boost, in addition to a FF boost due to sidewall passivation. There is virtually no change in cell parameters. This is particularly noteworthy for the Voc and FF, both of which are increasingly at risk to possible enhanced depletion region recombination and shunting via microcracks and TDD pileups as area is increased. The fact that there is no area dependence indicates that no fundamental barriers exist for achieving cell areas that are compatible with current applications. To our knowledge, the 4 cm^2 cell area is more than 10x larger than any prior U.S. epitaxial GaAs/Si cell with reasonable performance and this is the first GaAs/Si approach cell to demonstrate no degradation with area scale up. Based on our earlier work, the projected AM0 efficiency after AR coating (uncoated AM0 values are shown in the inset) for the 4 cm^2 cell will increase to ~ 14%, which would be ~ 16% under AM1.5 illumination. It is worth noting that the TDD for the v-Ge substrates used here were ~ 2x higher than those that yielded Voc values of 980 mV and AM0 efficiencies of 15.6% for 0.04 cm^2 cells (17.1% with active GaAs/v-Ge interface). Large area cells on lower TDD substrates are being developed now that we have achieved a significant scale up in GaAs area on Si.

4. Summary

Significant progress on developing GaAs/SiGe/Si cells has been made on three fronts that will guide further research and development of GaAs/v-Ge photovoltaics toward multi-junction III-V cell integration with Si. First, a preferred polarity for III-V cells in the presence of low, but non-negligible TDD values has been discovered, with p^+n cells being far less sensitive to TDD than n^+p cells. Second, a method to control inadvertent GaAs/Ge interface electrical activity for III-V cells grown on v-Ge has been achieved for p^+n configured cells, and the source for such activity is suggested to be impurity-related. Third, GaAs/Si cell areas have been increased to 4 cm^2 with no impact on cell performance by using graded SiGe buffers on Si.

4. Acknowledgements

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